REMARKS/ARGUMENTS

Claims 1-35 remain in this application. Claims 1, 5, and 22-32 are amended to more distinctly describe the subject matter of applicant's invention and to correct a typographical error in claim 5 as filed. Claims 33-35 are amended to more distinctly describe the invention. No new matter is added by these amendments and the amendments are not intended to affect the scope of the claims.

A. Rejections under 35 U.S.C. 112

Claims 23-32 were rejected under 35 U.S.C. 112. This rejection is respectfully traversed. Claim 22 is amended to clarify the distinction between the two circuits that appeared in the claim as filed. Corresponding amendments are made to claims 23-32. These amendments are believed to overcome the rejection to claims 22-32.

B. Rejections under 35 U.S.C. 102

Claims 1-6, 11-13, 15-18, 20-22 and 25-34 were rejected under 35 U.S.C. 102 as anticipated by Wolff et al. This rejection is respectfully traversed.

Independent claims 1, 22, 33 and 34 call for, in varying language, monitoring packet information on an interconnect. At least this feature of the independent claims is not shown or suggested in the Wolff et al. reference. Wolff et al. does not show or suggest using a packet interconnect. Wolff et al. contemplate monitoring a the signals that pass on an interconnect (see column 4, lines 64-68), but not packets. A common definition of a packet in a data communication network is: "A group of bits, including data and control elements that is switched and transmitted as a unit" (Modern Dictionary of Electronics, Sixth Ed., Howard W. Sams & Company, 1988). Nothing in Wolff et al. would suggest this packet feature of the instant claims.

Moreover, Wolff et al. do not monitor information from the interconnect as that term is used in the instant application. Wolff et al suggest monitoring the signals to detect error conditions, and suggest deriving parity information from the signals, but do not show or suggest directly monitoring the information itself. There is a

significant difference between monitoring signals for an error condition, and monitoring information contained within a packet as called for by independent claims 1, 22, 33 and 34. For at least these reasons, claims 1-6, 11-13, 15-18, 20-22 and 25-34 are believed to be allowable over Wolff et al.

C. Rejections under 35 U.S.C. 103

Claims 7-10 were rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Cepulis et al. This rejection is respectfully traversed. Claims 7-10 depend from claim 1 and are believed to distinguish over Wolff et al. for at least the same reasons as claim 1. Cepulis et al do not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

Claim 14 was rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Ardini, Jr. et al. This rejection is respectfully traversed. Claim 14 depends from claim 1 and is believed to distinguish over Wolff et al. for at least the same reasons as claim 1. The Ardini reference does not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

Claims 9 and 35 were rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Pizzicia. This rejection is respectfully traversed. Claims 9 depends from claim 1 and is believed to distinguish over Wolff et al. for at least the same reasons as claim 1. Pizzicia does not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

Claims 23 and 24 were rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Bershteyn et al. This rejection is respectfully traversed. Claims 23 and 24 depend from claim 22 and are believed to distinguish over Wolff et al. for at least the same reasons as claim 22. Bershteyn et al. do not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

D. Conclusion

In view of all of the above claims 1-35 are believed to be allowable and the case in condition for allowance which action is respectfully requested. The references

that were cited and not relied upon are believed to be no more pertinent that those references that were relied upon.

No fee is believed to be required by this response as determined on the accompanying transmittal letter. Should any other fee be required, please charge Deposit 50-1123. Should any extension of time be required please consider this a petition therefore and charge the required fee to Deposit Account 50-1123. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings To Show Changes Made**"

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

A. In the claims

1(Amended). In a system comprising an interconnect and a plurality of modules connected to said interconnect for putting packets of information onto the interconnect, wherein each packet comprises a number of fields containing information, a circuit comprising:

circuitry for receiving at least part [of said] of said information;

circuitry for determining if said at least part of said information satisfies one or more conditions; and

circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions.

5(Amended). A circuit as claimed in claim 1, wherein said action is to prevent one or more modules from being granted access to the interconnect.

22(Amended). A functional circuit comprising:

an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring information containing packets put onto the interconnect by one or more modules, said monitoring circuit comprising:

circuitry for determining if the information [on the interconnect] in a packet matches one or more conditions; and

circuitry for performing one or more actions if it is determined that information on the interconnect matches said one or more conditions.

23(Amended). A functional circuit as claimed in claim 22, wherein the functional circuit is an integrated circuit.

24(Amended). A functional circuit as claimed in claim [22] 23, wherein at least one module is external to said integrated circuit.

25(Amended). A functional circuit as claimed in claim 22, wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time.

26(Amended). A functional circuit as claimed in claim 25, wherein said determining circuitry is at least partially in the arbiter.

27(Amended). A functional circuit as claimed in claim 25, wherein said determining circuit does not delay the arbitration provided by the arbiter.

28(Amended). A functional circuit as claimed in claim 22, wherein said interconnect is a bus.

29(Amended). A functional circuit as claimed in claim 22, wherein one of said modules comprises a debug module.

30(Amended). A functional circuit as claimed in claim 29, wherein at least some of said circuitry for performing at least one action is in said debug module.

31(Amended). A functional circuit as claimed in claim 25, wherein at least some of said circuitry for performing at least one action is in said arbiter.

32(Amended). A functional circuit as claimed in claim 29, wherein at least part of the determining circuitry is in the debug module.

33(Amended). A method comprising the steps of:

monitoring information containing packets on an interconnect, the information being put onto the interconnect by one or modules;

determining if the information on an interconnect satisfies one or more conditions; and

carrying out one or more actions if it is determined that the information containing packet satisfies one or more conditions.

34(Amended). A circuit for monitoring packet information on an interconnect, said information being put onto the interconnect by one or more modules connected to

the interconnect, said circuit being arranged to determine if the information satisfies one or more conditions.

35(Amended). A circuit for monitoring packet information on an interconnect, said information being put onto the interconnect by one or more modules connected to the interconnect, said circuit being arranged to determine if the information satisfies one or more conditions and to select the information satisfying the one or more conditions.